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10/559,913	12/07/2005	Adrianus W.P.G.G. Vaassen	NL03 0686 US1	9556

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/559,913	VAASSEN, ADRIANUS W.P.G.G.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the papers filed on 4/13/09.

The previous rejection have been withdrawn in view of the amendment and remarks; however, new grounds of rejection have been cited in this office action in view of further consideration.

Claims 1-20 are pending.

Claim Objection

In claims 1 and 14, "a combine distance", as these claims presented, is unclear and incomplete as to "a combine distance" regarding what, i.e., "distance" regarding the length of power/ground buses/rails/conductors between power/ground pads or "a combine distance" regarding spacing between power/ground pads.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seefeldt (US patent 4,978,633) in view of at least one of: Hirakimoto (US pub. 2004/0031007) and Nassif (US pub. 2004/0073881)

Seefeldt discloses in fig. 3:

(Claim 1) An IC having a power distribution network, the power distribution network comprising:

A power bus and a ground bus (73 and 77) for supplying power from respective power and ground pads (71 and 75) to a plurality of circuit elements (cells 61-65) on the IC; and

Wherein the power distribution network is configured such that each given circuit element on the IC is arranged with a combined distance between the power pad and said circuit element, and between the ground pad and said circuit element, and each of the combined distances being equal.

(Taking cells 61 and 65 in fig. 3 as "each given circuit element" for illustration:

Cell 61 is arranged such that a distant from power pad 71 to cell 61 (let labeled short61 since cell 61 is placed closer to power pad 71) and distant from cell 61 to ground pad 75 (let labeled long61 since cell 61 is placed far away from ground pad 7);and
Let define: short61 + long61 = combined distance 61

Cell 65 is arranged such that a distant from ground pad 75 to cell 65 (let labeled short65 since cell 65 is placed closer to ground pad 75) and distant from cell 65 to power pad 71 (let labeled long65 since cell 65 is placed far away from power pad 71);and
Let define: short65 + long65 = combined distance 65.

Thus, according to above interpretation together with the layout in fig 3 shown as proof and evident, combined distance 61for cell 61 as defined equal combined distance 65 for cell 65with respect to fig 3. This proves the combined distance for each cells 61-65 to power and ground pads being equal due to ***complementary factor****, for example, short complemented by long and vice versa, long complemented by short or in other words, a length decreased of power/ground line (conductor/bus) from a power/ground pad complemented by a length increased of ground/power line (conductor/bus) from a ground/power pad, no matter where these cells 61-65 are placed/located in the IC. These Features of the prior art correspond to claims14-15 and fig 3 of the instant Application.*

Further explanation as to why the prior art design/IC constitute combined distance for each cells 61-65 to power and ground pads being equal are:

a. ***Power pad and ground pad are arranged at diagonally opposite corners*** *of IC and power buses and wires are then routed to cells 61-65 from power/ground pads as shown in prior art fig 3 (that corresponds to fig 3 and claim 3 of the instant application); and*

b. ***Complementary factor*** *as explained above*

Thus, Seefeldt discloses substantially all the elements in claim 1 except the decoupling cells in claim 1; however,

Nassif discloses decoupling cells (DECAPs) in fig. 4

Hirakimoto discloses decoupling cells (CAPACITIVE CELLS) in par 118, 141.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize decoupling cells **simply because at least one of the following reasons**:

As disclosed by Nassif: "*using decoupling capacitors to reduce noise in an integrated circuit*" (par 2); "*the use of decap is well-known in the art*" (par 10); and "*utilizes decoupling capacitors in the power grid to reduce power supply induced noise*" (par 13, 31).

As disclosed by Hirakimoto, capacitive cells "to *provide a steady power supply voltage and a negative effect of noise of power supply, ground and the like can be eliminated/prevented*" (par 118, 141).

(Note that the claim limitation "decoupling cell for providing static current" between power and ground is an inherent function of decaps in Nassif reference and an inherent function of capacitive cells in Hirakimoto reference (also an inherent function for any capacitor/decap/cap cells that is used for power *decoupling* purpose (also called (power) by-passing capacitors)) since capacitors in both Nassif and Hirakimoto are used for decoupling/bypass application and placed between power and ground and connected to power and ground to provide "*a steady power supply voltage*")

(Claim 2) wherein the combined distances are equal for predominantly all of the circuit elements (cells 61-65 in fig 3 of Seefeldt) in the IC

(Claim 3) wherein the power pad and the ground pad (71 and 75 in fig 3 of Seefeldt) are arranged at diagonally opposite corners of the IC.

(Claim 4) wherein the power distribution network comprises: (see Seefeldt fig 3)

A power bus comprising a vertical section (81 and/or 83) connected to the power pad (71), and one or more horizontal sections (73) connected to the vertical section;

A ground bus comprising a vertical section (82 and/or 84) connected to the ground pad (75) and one or more horizontal sections (77) connected to the vertical section;

wherein the vertical section (81 and/or 83) of the power bus is arranged parallel to the vertical section (82 and/or 84) of the ground bus, such that the one or more horizontal sections of the power bus interleave the one or more horizontal sections of the ground bus (as shown in fig 3) and wherein one of the circuit elements (i.e., cell 61) is connected between horizontal sections of the power bus and ground bus and arranged with said

combined distance that is equal to said combined distance for another one (i.e., cell 65) of the circuit elements that is connected between different horizontal sections of the power bus and ground bus.

(Claim 5) wherein a horizontal section of the power bus and a horizontal section of a ground bus form a row for powering one or more of the circuit elements (fig 3 and related text shown/disclosed row power and ground rail/buses/trunk/grid/wire to power cells 61-65).

(Claim 6) wherein one or more circuit elements (cells 61-65) are located between the horizontal sections of the power bus (73) and the horizontal section of the ground bus (77).

(Claim 7) wherein the decoupling cells (both DECAPs in fig. 4 of Nassif and CAPACITIVE CELLS in par 118, 141 of Hirakimoto) include decoupling capacitors

(Claim 8) wherein the decoupling cells are configured to be the same height as the circuit elements (both fig 4 of Nassif show DECAPs 70 configured to be the same height as the circuit elements (cell 68) and fig 8A-B of Hirakimoto shown CAPACITIVE CELLS configured to be the same height as the circuit elements (macrocells, cells))

(Claim 9) wherein the decoupling cells are arranged between circuit elements on IC (both fig 4 of Nassif show DECAPs 70 are arranged between the circuit elements (cells 68) and fig 8A-B of Hirakimoto shown CAPACITIVE CELLS arranged between the circuit elements (cells, macrocells))

(Claim 10) wherein the power distribution network comprises one or more smaller power distribution networks having the same configuration (Seefeldt fig 3 and corresponding text shows/discloses power/ground pads connected to big power/ground busses and the power/ground busses split to multiple smaller networks with small power/ground conductors/lines/tracks having similar configuration distributing power to cells)

(Claim 11) wherein the power distribution network is configured to maintain the voltage drop between the power pad and each circuit element constant, relative to the voltage drop for predominantly all of the circuit elements in the IC (in Seefeldt fig 3, the symmetrical layout with opposite corner of power and ground pad and symmetrically

similar configuration layout of power/ground inherently maintain the voltage drop between the power pad and each circuit element constant)

(Claim 12) wherein the decoupling cells are configured to maintain the voltage drop between the power pad and each circuit element constant, relative to the voltage drop for predominantly all of the circuit elements in the IC (Both: at least par 52 of Nassif and at least the abstract of Hirakimoto disclose this limitation).

(Claim 13) wherein the decoupling cells are configured to selectively couple each of said given circuit elements to maintain combined distance constant among predominantly all of the circuit elements (Fig 4 of Nassif and corresponding text shows and discloses decoupling cells (DECAPs 70) are configured to selectively couple each of said given circuit elements (cells 68) to maintain combined distance constant among predominantly all of the circuit elements. Fig 11 of Hirakimoto also discloses decoupling cells (CAPACITIVE CELLS) are configured to selectively couple each of said given circuit elements (cells, Macrocells) to maintain combined distance constant among predominantly all of the circuit elements).

Claims 14-20 recited similar subject matter and the same rejection applied.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pryor (US patent 4,612,618) in view of at least one of: Hirakimoto (US pub. 2004/0031007) and Nassif (US pub. 2004/0073881)

Pryor discloses in "PRIOR ART" fig. 3:

(Claim 1) An IC having a power distribution network, the power distribution network comprising:

A power bus (125) and a ground bus (123) for supplying power from respective power and ground pads (*pads 124P and 122P, note that fig 3 labeled pads 124P and 122P as V2 and V1, respectively. V2 and V1 are inherently power and ground, respectively or ground and power, respectively to provide power to circuit cells 10 which are logic circuits, logic gates, logic cells. For interpretation, the Examiner considers V1 and V2 as ground and power, respectively*) to a plurality of circuit elements (cells 10) on the IC; and

Wherein the power distribution network is configured such that each given circuit element on the IC is arranged with a combined distance between the power pad and said circuit element, and between the ground pad and said circuit element, and each of the combined distances being equal.

(As shown in fig 3:

Pads 122P and 124P are for V1 and V2 representing ground and power respectively. V1 and V2 connected to ground bus 123 and power bus 125, respectively.

V1 and V2 and bus 123, 125 are then split to horizontal and vertical power trace/stripes/rails/wires and horizontal and vertical ground trace/stripes/rails/wires (22, 24, 122, 124, 122H and 124H) wherein row power and ground buses 22 and 24 extend along each row 140 of cells 10 to supply power to cells 10.

In "PRIOR ART" fig 3 of Pryor, the power layout is symmetrical with ***power and ground pads (P124P and 122P) are positioned at diagonally opposite corners. "PRIOR ART" fig 3 in reference Pryor corresponds to fig 3 and claim 3 of the Applicant Application***

Using similar interpretation/explanation as detailed in reference Seefeldt; it is the symmetrical power layout in fig 3 of Pryor with power and ground pads (P124P and 122P) positioned at diagonally opposite corners and the power routing distribution of trace/stripes/rails/wires (22, 24, 122, 124, 122H and 124H) that provide ***complementary factor (as explained above)*** *such that each given circuit element (cells 10) on the IC is arranged with a combined distance between the power pad (124P) and said circuit element (cells 10), and between the ground pad (122P) and said circuit element (cells 10), and each of the combined distances being equal)*

Thus, Pryor discloses substantially all the elements in claim 1 except the decoupling cells in claim 1; however,

Nassif discloses decoupling cells (DECAPs) in fig. 4

Hirakimoto discloses decoupling cells (CAPACITIVE CELLS) in par 118, 141.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize decoupling cells simply because at least one of the following reasons:

As disclosed by Nassif: "*using decoupling capacitors to reduce noise in an integrated circuit*" (par 2); "*the use of decap is well-known in the art*" (par 10); and "*utilizes decoupling capacitors in the power grid to reduce power supply induced noise*" (par 13, 31).

As disclosed by Hirakimoto, capacitive cells "to *provide a steady power supply voltage and a negative effect of noise of power supply, ground and the like can be eliminated/prevented*" (par 118, 141).

(Note that the claim limitation "decoupling cell for providing static current" between power and ground is an inherent function of decaps in Nassif reference and an inherent function of capacitive cells in Hirakimoto reference (also an inherent function for any capacitor/decap/cap cells that is used for power *decoupling* purpose (also called (power) by-passing capacitors)) since capacitors in both Nassif and Hirakimoto are used for decoupling/bypass application and placed between power and ground and connected to power and ground to provide "*a steady power supply voltage*")

(Claim 2) wherein the combined distances are equal for predominantly all of the circuit elements (cells 10 in cell row 140 in fig 3 of Pryor) in the IC

(Claim 3) wherein the power pad and the ground pad (124P and 122P in fig 3 of Pryor) are arranged at diagonally opposite corners of the IC.

(Claim 4) wherein the power distribution network comprises: (see Pryor fig 3)

A power bus comprising a vertical section (124) connected to the power pad (124P), and one or more horizontal sections (22) connected to the vertical section;

A ground bus comprising a vertical section (122) connected to the ground pad (122P) and one or more horizontal sections (24) connected to the vertical section;

wherein the vertical section (124) of the power bus is arranged parallel to the vertical section (122) of the ground bus, such that the one or more horizontal sections of the power bus interleave the one or more horizontal sections of the ground bus (as shown in fig 3) and wherein one of the circuit elements (i.e., cell 10) is connected between horizontal sections of the power bus and ground bus and arranged with said combined distance that is equal to said combined distance for another one (i.e., cell 65) of the circuit elements that is connected between different horizontal sections of the power bus and ground bus.

(Claim 5) wherein a horizontal section of the power bus and a horizontal section of a ground bus form a row for powering one or more of the circuit elements (see Pryor col 4 lines 43-46).

(Claim 6) wherein one or more circuit elements (Pryor cells 10 in fig 3) are located between the horizontal sections of the power bus (125 and/or 24) and the horizontal section of the ground bus (123 and/or 22).

(Claim 7) wherein the decoupling cells include decoupling capacitors (both DECAPs in fig. 4 of Nassif and CAPACITIVE CELLS in par 118, 141 of Hirakimoto include decoupling capacitors)

(Claim 8) wherein the decoupling cells are configured to be the same height as the circuit elements (both fig 4 of Nassif show DECAPs 70 configured to be the same height as the circuit elements (cell 68) and fig 8A-B of Hirakimoto shown CAPACITIVE CELLS configured to be the same height as the circuit elements (macrocells, cells))

(Claim 9) wherein the decoupling cells are arranged between circuit elements on IC (both fig 4 of Nassif show DECAPs 70 are arranged between the circuit elements (cells 68) and fig 8A-B of Hirakimoto shown CAPACITIVE CELLS arranged between the circuit elements (cells, macrocells))

(Claim 10) wherein the power distribution network comprises one or more smaller power distribution networks having the same configuration (Pryor fig 3 and corresponding text shows/discloses power/ground pads (122P, 124P) connected to big power/ground busses and the power/ground busses split to multiple smaller networks with small power/ground conductors/lines/tracks having similar configuration distributing power rows 140 to cells 10)

(Claim 11) wherein the power distribution network is configured to maintain the voltage drop between the power pad and each circuit element constant, relative to the voltage drop for predominantly all of the circuit elements in the IC (in Pryor fig 3, the symmetrical layout with opposite corners of power and ground pads and symmetrically similar configuration layout of power/ground inherently maintain the voltage drop between the power pad and each circuit element constant)

(Claim 12) wherein the decoupling cells are configured to maintain the voltage drop between the power pad and each circuit element constant, relative to the voltage drop for predominantly all of the circuit elements in the IC (Both: at least par 52 of Nassif and at least the abstract of Hirakimoto disclose this limitation).

(Claim 13) wherein the decoupling cells are configured to selectively couple each of said given circuit elements to maintain combined distance constant among predominantly all of the circuit elements (Fig 4 of Nassif and corresponding text shows

and discloses decoupling cells (DECAPs 70) are configured to selectively couple each of said given circuit elements (cells 68) to maintain combined distance constant among predominantly all of the circuit elements. Fig 11 of Hirakimoto also discloses decoupling cells (CAPACITIVE CELLS) are configured to selectively couple each of said given circuit elements (cells, Macrocells) to maintain combined distance constant among predominantly all of the circuit elements).

Claims 14-20 recited similar subject matter and the same rejection applied.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
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